ABSTRACT OF THE DISCLOSURE

The present invention is intended to provide a delay lock loop circuit which is capable of providing a minute delay amount with stability regardless of the variations in delay amount due to variations in temperature and power supply voltage for example and process conditions. On the basis of a up/down control signal from a delay amount detector, count value is counted from initial setting value up to maximum setting value or down to minimum setting value. When the count value has reached the maximum or minimum value, another count value is counted up and down, thereby cutting the noise component of the up/down control signal. Consequently, regardless of the variation in delay amount due to a delay line, a delay lock detector to which the latter count value is supplied operates normally, thereby outputting with stability a reference delay step count for obtaining a delay of 1T.